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PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8021
SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8-Bit CPU, ROM, RAM, I/O in Single 28-Pin Package**
- **Single 5V Supply (+4.5V to 6.5V)**
- **8.38 μsec Cycle With 3.58 MHz XTAL; All Instructions 1 or 2 Cycles**
- **Instructions —8748 Subset**
- **High Current Drive Capability—2 Pins**
- **1K × 8 ROM**
  64 × 8 RAM
  21 I/O Lines
- **Interval Timer/Event Counter**
- **Clock Generated With Single Resistor or Inductor**
- **Zero-Cross Detection Capability**
- **Easily Expandable I/O**

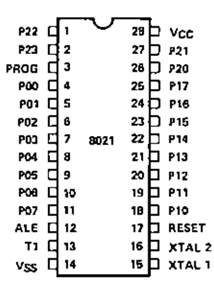
The Intel® 8021 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process. The features of the 8021 include a subset of the 8048 optimized for low cost, high volume applications, plus additional I/O flexibility and power.

The 8021 contains a 1K X 8 program memory, a 64 X 8 data memory, 21 I/O lines, and an 8-bit timer/event counter, in addition to on-board oscillator and clock circuits. For systems that require extra I/O capability, the 8021 can be expanded using the 8243 or discrete logic.

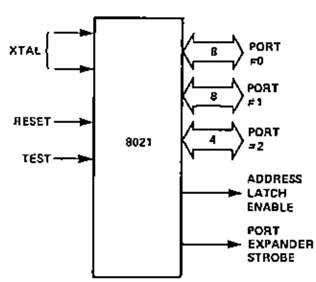
This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8021 has bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

To minimize development problems and maximize flexibility, an 8021 system can be easily designed using the 8021 emulation board, EMB-21. The EMB-21 contains a 40-pin socket which can accommodate either the 8748 shipped with the board or an ICE-48 plug. Also, the necessary discrete logic to reproduce the 8021's additional I/O features is included.

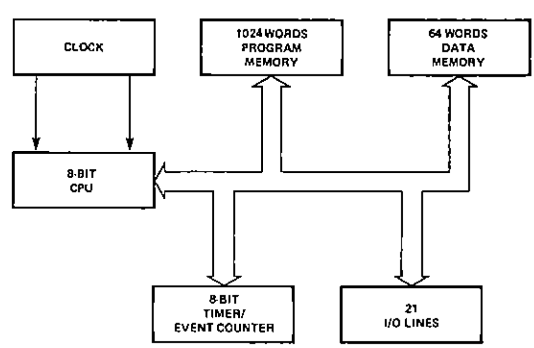
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . −0.5V to +7V
Power Dissipation . . . . 1 W

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage (All except XTAL1, XTAL2)	-0.5		0.8	V	
V_{IH}	Input High Voltage (All except XTAL1, XTAL2)	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH_1}	Input High Voltage (All except XTAL1, XTAL2)	3.0		V_{CC}	V	$V_{CC} = 5.5V \pm 1V$
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6$ mA
V_{OL_1}	Output Low Voltage (P10, P11)			2.5	V	$I_{OL} = 7$ mA
V_{OH}	Output High Voltage (All unless Open Drain)	2.4			V	$I_{OH} = 50\ \mu A$
I_{OL}	Output Leakage Current (Open Drain Option — Port 0)			±10	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
I_{CC}	V_{CC} Supply Current			100	mA	

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CY}	Cycle Time	8.38	50.0	μsec	3 MHz XTAL = 10 μsec t_{CY}
Δ_F	Oscillator Frequency Variation -Resistor Mode	−20	+20	%	F = 2.5 MHz

A.C. TEST CONDITIONS

Control Outputs: $C_L = 80$ pF

MCS-48

PRELIMINARY

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MCS-48

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	14	Circuit GND potential
V_{CC}	28	+5V power supply
PROG	3	Output strobe for 8243 I/O Expander
P00–P07 Port 0	4–11	8-bit quasi-bidirectional port
P10–P17 Port 1	18–25	8-bit quasi-bidirectional port
P20–P23 Port 2	26–27 1–2	4-bit quasi-bidirectional port P20–P23 also serve as a 4-bit I/O expander bus for 8243
T1	13	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/event counter input using the STRT CNT instruction. Also allows zero-crossover sensing of slowly moving AC inputs.
RESET	17	Input used to initialize the processor by clearing status flip-flops and setting program counters to zero.
ALE	12	Address Latch Enable. Signal occuring once every 30 input clocks, used as an output clock.
XTAL1	15	One side of crystal, inductor, or resistor input for internal oscillator. Also input for external source. (Not TTL compatible.)
XTAL2	16	Other side of timing control element.

INSTRUCTION SET*

Group	Mnemonic		Description	Bytes	Cycle
Accumulator	ADD	A,R	Add register to A	1	1
	ADD	A,@R	Add data memory to A	1	1
	ADD	A,#data	Add immediate to A	2	2
	ADDC	A,R	Add with carry	1	1
	ADDC	A,@R	Add with carry	1	1
	ADDC	A,#data	Add with carry	2	2
	ANL	A,R	And register to A	1	1
	ANL	A,@R	And data memory to A	1	1
	ANL	A,#data	And immediate to A	2	2
	ORL	A,R	Or register to A	1	1
	ORL	A,@R	Or data memory to A	1	1
	ORL	A,#data	Or immediate to A	2	2
	XRL	A,R	Exclusive Or register to A	1	1
	XRL	A,@R	Exclusive or data memory to A	1	1
	XRL	A,#data	Exclusive or immediate to A	2	2
	INC	A	Increment A	1	1
	DEC	A	Decrement A	1	1
	CLR	A	Clear A	1	1
	CPL	A	Complement A	1	1
	DA	A	Decimal Adjust A	1	1
	SWAP	A	Swap nibbles of A	1	1
	RL	A	Rotate A left	1	1
	RLC	A	Rotate A left through carry	1	1
	RR	A	Rotate A right	1	1
	RRC	A	Rotate A right through carry	1	1
Input/Output	IN	A,P	Input port to A	1	2
	OUTL	P,A	Output A to port	1	2
	MOVD	A,P	Input Expander port to A	1	2
	MOVD	P,A	Output A to Expander port	1	2
	ANLD	P,A	And A to Expander port	1	2
	ORLD	P,A	Or A to Expander port	1	2
Registers	INC	R	Increment register	1	1
	INC	@R	Increment data memory	1	1
Branch	JMP	addr	Jump unconditional	2	2
	JMPP	@A	Jump indirect	1	2
	DJNZ	R,addr	Decrement register and Jump on R not zero	2	2
Branch	JC	addr	Jump on Carry = 1	2	2
	JNC	addr	Jump on Carry = 0	2	2
	JZ	addr	Jump on A Zero	2	2
	JNZ	addr	Jump on A not Zero	2	2
	JT1	addr	Jump on T1 = 1	2	2
	JNT1	addr	Jump on T1 = 0	2	2
	JTF	addr	Jump on timer flag	2	2
Subroutine	CALL	addr	Jump to subroutine	2	2
	RET		Return	1	2
Flags	CLR	C	Clear Carry	1	1
	CPL	C	Complement Carry	1	1
Data Moves	MOV	A,R	Move register to A	1	1
	MOV	A,@R	Move data memory to A	1	1
	MOV	A,#data	Move immediate to A	2	2
	MOV	R,A	Move A to register	1	1
	MOV	@R,A	Move A to data memory	1	1
	MOV	R,#data	Move immediate to register	2	2
	MOV	@R,#data	Move immediate to data memory	2	2
	XCH	A,R	Exchange A and register	1	1
	XCH	A,@R	Exchange A and data memory	1	1
	XCHD	A,@R	Exchange nibble of A and register	1	1
	MOVP	A,@A	Move to A from current page	1	2
Timer/Counter	MOV	A,T	Read Timer/Counter	1	1
	MOV	T,A	Load Timer/Counter	1	1
	STRT	T	Start Timer	1	1
	STRT	CNT	Start Counter	1	1
	STOP	TCNT	Stop Timer/Counter	1	1
	NOP		No Operation	1	1

*See July, 1978 MCS-48 User's Manual for opcodes.

FUNCTIONAL SPECIFICATIONS

The following is a functional description of the major elements of the 8021.

Program Memory

The 8021 contains 1K X 8 of mask programmable ROM. No external ROM expansion capability is provided.

Data Memory

A 64 X 8 dynamic RAM is located on chip for data storage. All locations are indirectly addressable and eight designated locations are directly addressable. Also, included in the memory is the address stack, addressed by a 3-bit stack pointer.

Memory is organized as shown in Figure 1. The least significant 8 addresses, 0–7, are directly addressable by any of the 11 direct register instructions. The locations are readily accessible for a variety of operations with the least number of instruction bytes required for their manipulation.

Registers 0 and 1 have yet another function, in that they can be used to indirectly address all locations in memory, using the indirect register instructions. These indirect RAM address registers, IRAR's, are especially useful for repetitive-type operations on adjacent memory locations. The indirect register instruction specifies which IRAR to use, and the contents of the IRAR is used to address a location in RAM. The contents of the addressed location is used during the execution of the instruction, and may be modified. A value larger than 63 should not be preset in the IRAR when selected by an indirect register instruction. IRAR's may point to addresses 0–7, if desired.

Locations 8–23 may be used as the address stack. The address stack enables the processor to keep track of the return addresses generated from CALL instructions. A 3-bit stack pointer (SP) supplies the address of the locations to be loaded with the next return address generated. The SP to this pushdown stack is incremented by one after a return address is stored, and decremented by one before an address is fetched during a RET. A total of 8 levels of nesting is possible. The SP is initialized to location 8 upon RESET. Since each address is 10 bits long, two bytes must be used to store a single address. The SP is incremented and decremented by one, but each increment or decrement moves the address pointed to by two. Therefore, only even numbered addresses are pointed to.

If a particular application does not require 8 levels of nesting, the unused portion of the stack may be used as any other indirectly addressable scratchpad location. For example, if only 3 levels of subroutine nesting are used, then only locations 8–15 need be reserved for the address stack, and locations 16–63 can be used for data storage. The actual program counter address is not stored in the address stack. A separate register retains its value.

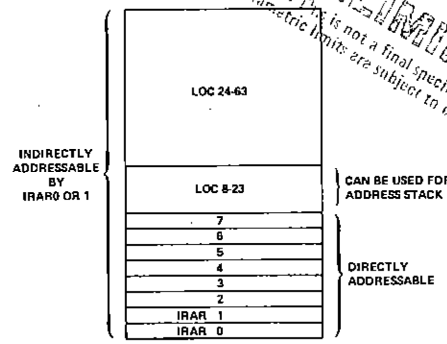

Figure 1. Internal RAM Organization

Oscillator and Clock

The 8021 contains its own onboard oscillator and clock circuit, requiring only an external timing control element. This control element can be a crystal, inductor, resistor, or clock in. The capacitor normally required in resistor or inductor timing control operation is integrated onto the 8021. All internal time slots are derived from the external element, and all outputs are a function of the oscillator frequency. Pins X1 and X2 are used to input the particular control element. An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods. Therefore, to obtain a 10 μsec instruction cycle, a 3 MHz crystal should be used.

Timer/Event Counter

An interval timer is available to enable the user to keep track of time elapsed or number of events occurred, during normal program execution and flow.

By a MOV T,A instruction, the contents of the accumulator are loaded to the timer. At the STRT T command an internal prescaler is zeroed and thereafter increments once each 30 input clocks (once each single cycle instruction, twice each double cycle instruction). The prescaler is a divide by 32. At the (11111) to (00000) transition the timer is incremented. The timer is 8 bits and an overflow (FFH) to (00H) timer flag is set. A conditional branch is available for testing this flag, the flag being reset each test. Total count capacity for the timer is $2^8 \times 2^5 = 8192$ or 81.9 msec at a 10 μsec cycle time. Contents of the timer are moved to the accumulator by the MOV A,T instruction without disturbing the counting process.

The timer may also be used as an event counter. After a STRT CNT command, the chip will respond to a high to low transition on the Test 1 pin by incrementing the timer. Transitions can occur no faster than one each three instruction cycles.

The timer and event functions are exclusive. Counting or timing may be started or stopped (STOP TCNT) at will.

Input/Output Capabilities

The 8021 I/O configurations are highly flexible. A number of different configurations are possible, tailoring an 8021 to a given task. Other than the power supply and dedicated pins, all other pins (20) can be used for input, output, or both, depending on the configuration.

P20–P23 and P10–P17 are quasi-bidirectional, and Test 1 is directly testable through program control. A simplified schematic of the quasi-bidirectional interface is shown in Figure 2. This configuration allows buffered outputs, and also allows external input. When writing a "0" or low value to these ports, the large pulldown device sinks an external TTL load. When writing a "1", a large current is supplied through the large pullup device to allow a fast data transfer. After a short time (less than one instruction cycle), the large device is shut off and the small pullup maintains the "1" level indefinitely. However, in this situtation, an input device capable of overriding the small amount of sustaining current supplied by the pullup device can be read. (Alternatively, the data written can be read). So, by writing a "1" to any particular pin, that pin can serve either as a true high-level latched output pin, or as just a pullup resistor on an input. This allows maximum user flexibility in selecting his input or latched output pins, with a minimum of external components.

Port 00–07 is also quasi-bidirectional, except there is no large pullup device. As outputs, this port is essentially open drain.

By mask option the small pullup devices on P00–P07 may be deleted on any pin providing a true open drain output. This is useful in driving analog circuits and certain loads, such as keyboards.

Also available is the 8243 I/O expander chip, which provides additional I/O capability with a limited number of overhead pins. This chip has 4 directly addressable 4-bit ports. It connects to the PROG pin, which provides a clock, and pins P20–P23, which provide address and data. These ports can be written with a MOVD P,A; ANLD P,A; and ORLD P,A for Ports 4–7. A high to low transition on PROG signifies that address and control are available on P20–P23. The previous data on P20–P23 before an output expander instruction is lost. Therefore, when using an output expander P20–P23 are not useful for general input/output. Reading is via the MOVD A,P. This circuit configuration is shown in Figure 3.

The Test 1 pin has a special bias input that allows zero-crossover sensing of slowly moving inputs. This is especially useful in SCR control of 60 Hz power and in developing time of day routines. As a ROM mask option there is a pullup resistor that is useful for switch contact input or standard TTL. See Figure 4.

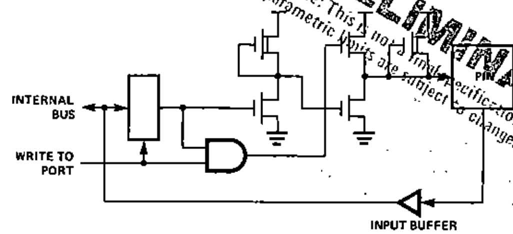

Figure 2. Quasi-Bidirectional Port Structure

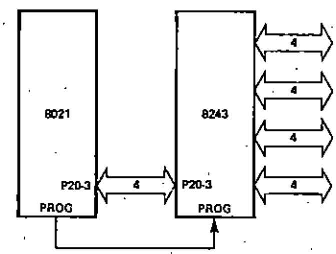

Figure 3. I/O Expander Interface

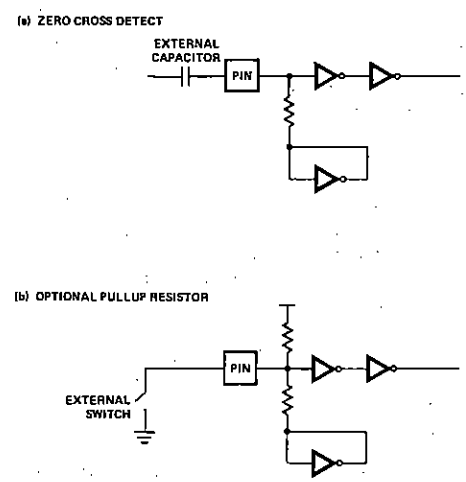

Figure 4. Test 1 Pin

CPU

The 8021 CPU has arithmetic and logical capability. A wide variety of arithmetic and logic instructions may be exercised, which affect the contents of the accumulator, and/or direct or indirect scratchpad locations. Provisions have been made for simplified BCD arithmetic capability through the use of the DAA, SWAP A, and XCHD instructions. In addition, MOVP A,@A allows table lookup for display formating and constants. Jump conditions such as zero, not zero refer to the accumulator contents at the time of the condition.

Reset

The 8021 may see poorly regulated and noisy power supplies. A useful feature is to sense when the power supply dips and do a reset to prevent continued operation with incorrect data. This feature may be implemented on the 8021 by connecting a diode between the RESET node and ground. See Figure 5.

A reset will then be forced if the supply drops approximately 1.5 volts and rapidly recovers. One instruction cycle will reset the 8021 to the initialized state.

By removing the diode and using only the capacitor, voltage drops in V_{CC} will not cause a RESET.

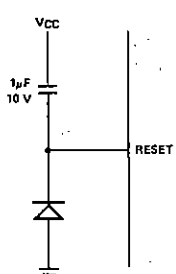

FIGURE 5. POWER ON RESET

Differences Between the 8021 and the 8748

Although the 8021 is basically an electrical and functional subset of the 8748, there are some differences:

1. *Pin Out* — As the 8021 is a 28-pin DIP, some form of adapter must be used to interface the 8021 socket to ICE-48. An emulation board, EM-1, has been designed to perform this function. The EM-1 also accounts for the increased flexibility of some 8021 I/O lines.
2. *Instruction Time* — The 8021 instruction cycle is 30 clock cycles long, the 8748 instruction cycle is 15 clocks long. Where exact timing is important the 8748 breadboard part should be operated at half the 8021 clock rate.
3. *Test 1* — To facilitate developing time of day routines from 60 Hz, and for SCR control, the Test 1 pin without the pullup resistor option will detect zero crossing of a capacitively coupled AC input.
4. *Quasi-Bidirectional Ports* — All 8021 ports are quasi-bidirectional to facilitate stand-alone use. Port 0 has open drain outputs and by mask option it may or may not have pullup resistors.
5. *Oscillator* — The 8021 has on-chip oscillator that is optimized for the single resistor mode. External connection will differ from the 8748.
6. *Dynamic RAM and Logic* — The 8021 utilizes dynamic RAM and some dynamic logic. Input clocking must be maintained above the minimum rate or improper operation may result.
7. *High Current Outputs* — Very high current drive is desirable for minimizing external parts required to do high power control. P10 and P11 have been designated high drive outputs capable of sinking 7 mA at V_{SS} +2.5 volts. (For clarity, this is 7 mA to V_{SS} with a 2.5 volt drop across the buffer.) These pins may, of course, be paralleled for 14 mA drive if the output logic states are always the same.
8. *Reset* — Reset has been modified on the 8021, as previously noted. A reset will be forced if the power supply drops approximately 1.5 volts and rapidly recovers, if a diode is used in the reset circuit. This prevents continued operation with incorrect data caused by a poorly regulated and/or noisy power supply.
9. *Instruction Set* — The following instructions, which are found in the 8748, have been deleted from the 8021 instruction set.

Data Moves	Registers	Branch	Timer	Control	Input/Output
MOV A,PSW	DEC R	JT0 addr	EN TCNTI	EN I	ANL P,#data
MOV PSW,A		JNT0 addr	DIS TCNTI	DIS I	ORL P,#data
MOVX A,@R	**Flags**	JF0 addr		SEL RB0	INS A,BUS *
MOVX @R,A	CLR F0	JF1 addr	**Subroutine**	SEL RB1	OUTL BUS,A *
MOVP3 A,@A	CPL F0	JNI addr	RETR	SEL MB0	ANL BUS,#data
	CLR F1	JBb addr		SEL MB1	ORL BUS,#data
	CPL F1			ENT0 CLK	

*These Instructions have been replaced in the 8021 by IN A,PO and OUTL PO,A respectively.

MCS-48

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